DROs, Part 3

EVALUATE DRO NOISE AND TUNING CHARACTERISTICS

Center frequency, temperature stability, phase noise, and frequency tuning are some key requirements in DRO designs.

TRANSISTOR dielectric resonator oscillators (DROs), which span the frequency range of 3 to 40 GHz, are available with power outputs ranging to greater than +23 dBm at X-band. As noted earlier, the oscillator can use either a silicon bipolar or GaAs FET device, each device having associated tradeoffs in performance. The oscillator can be followed by one or more buffer amplifier stages that are required to meet power-output specifications.

A DRO's center frequency can be fixed or tuned over a narrow band by mechanical or electrical means. A DRO's center frequency is usually specified in terms of MHz, with a specified frequency accuracy that is dependent upon variations with temperature, load (pulling), supply voltage (pushing), time (aging), and settability. (For more details on DRO characterization, consult Avantek Application Note AN-M004.)

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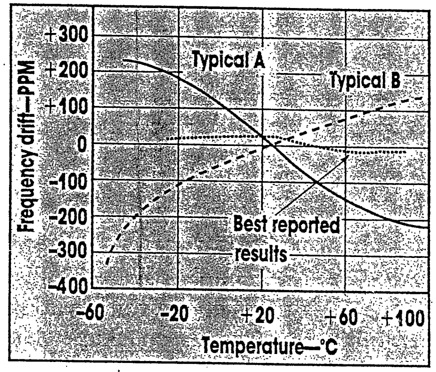

1. A 12-GHz DRO can exhibit a wide range of frequency drift at temperatures from -60 to +100°C.

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Temperature stability is the measure of the change in oscillator frequency over the specified temperature range. Traditionally, this has been expressed in parts per million per degree Celsius (PPM/°C). In general, the DRO frequency change is not a linear function of the temperature change, therefore, the frequency stability should be the maximum frequency change in percent (or PPM) with respect to the ideal frequency for a specified temperature range. For example, a typical 10-GHz DRO could have a frequency stability of ±500 PPM over -55 to +85°C. This specification implies that the DRO frequency will not drift more than 5 MHz on either side of 10 GHz over that temperature range.

The principal cause of DRO frequency drift with temperature is the phase deviation between the resonant circuit and the active circuit, including device circuitry, feedback circuitry, and output circuitry. Through the use of the oscillation condition in the reflection-coefficient form,[1] it can be easily proved that the temperature coefficient of DRO frequency is a function of the following parameters:

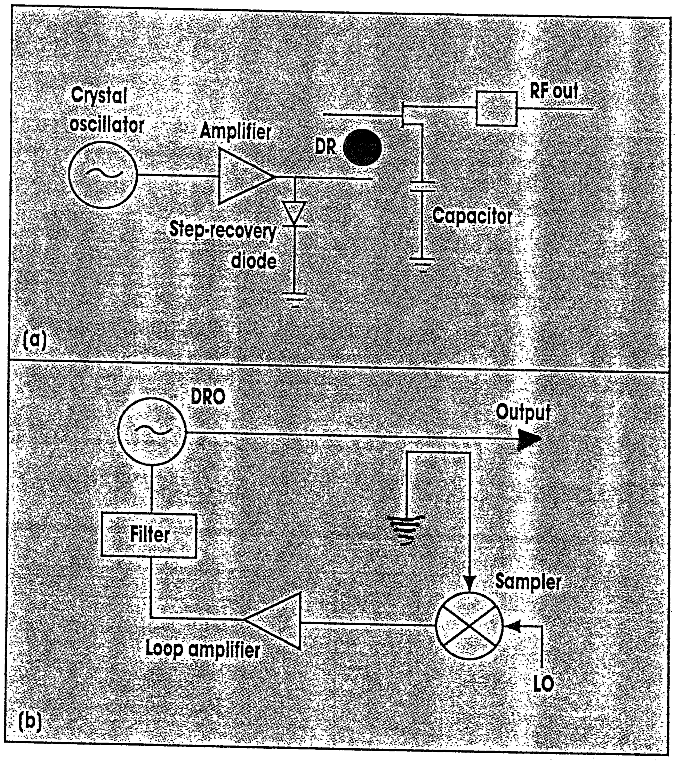
- the temperature coefficient, τ_f, of the dielectric resonator placed in a given shielded MIC configuration;
- the unloaded Q of the dielectric resonator;
- the coupling coefficient of the dielectric resonator with the microstrip line; and
- the temperature coefficient, τ_p, of the device (transistor) input reflection-coefficient phase that is known to decrease linearly with temperature change.

To construct a temperature-compensated DRO, a resonator with a temperature coefficient of +1 to +4 PPM/°C is generally required to offset the negative temperature coefficient of the device phase temperature coefficient (Fig. 1). With present technology, it is now possible to repeatably produce free-running DROs with a frequency drift of less than ±100 PPM over the -55 to +85°C military temperature range at frequencies to 18 GHz. However, results reported in the R&D environment are significantly better (±10 PPM over temperature).

TEMPERATURE STABILITY

Certain system applications require greater temperature stabilities than are possible using free-running DROs, even with temperature compensation. A number of techniques are used to improve the temperature stability of a DRO. The digitally-compensated DRO (DC-DRO) uses a sensor mounted in the oscillator to detect temperature changes. The output of the sensor goes through an analog-to-digital converter (ADC) to produce a digital word corresponding to the particular temperature. Electronically-programmable read-only memories (EPROMs), programmed with the temperature characteristics of the DRO and a correction look-up table, drive a digital-to-analog converter (DAC) to provide the correction signal, which is applied to the varactor diode of an electronically-tuned DRO (ET-DRO). Using this technique, frequency stability of ±15 PPM can be obtained over a wide temperature range.[2]

The analog-compensated DRO (AC-DRO) uses an analog compensator circuit in conjunction with a temperature sensor to achieve as much as ±20-PPM frequency stability. In analog compensation, the individual oscillator is tested to produce a custom tuning-voltage-versus-temperature curve, which is required to maintain a constant frequency. The compensation circuit is then aligned to fit the curve of the specific oscillator.



2. These simple architectures demonstrate an (a) injection-locked DRO and a (b) phase-locked DRO.

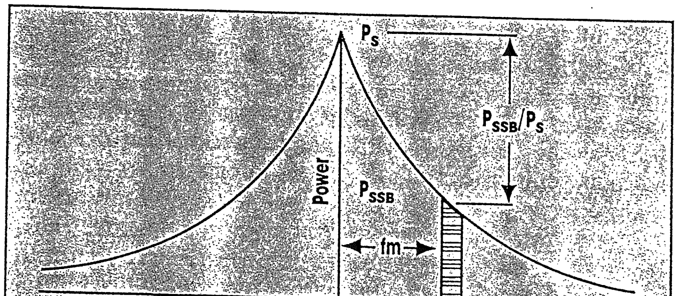
Ovenization may also be used to enhance the temperature stability of a DRO. To achieve temperature stability, the oscillator package is inserted in a temperature-stabilized oven. Using a heater element, a quick-response thermistor, and associated control circuitry, the package temperature can be maintained within ±5°C at 5 to 10°C above the maximum ambient temperature. A total frequency stability of better than ±10 PPM can be obtained with this approach.

Ovenized DROs offer lower phase noise than AC- or DC-DROs because the oscillator does not need to incorporate electrical tuning circuitry. AC- and DC-DROs, however, are smaller in size and do not need the substantial amount of heater power required by the ovenized DRO.

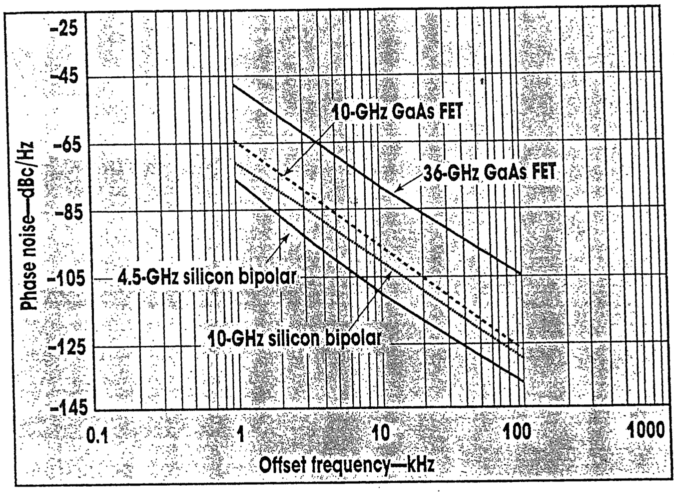
Phase-locked DROs (PL-DROs) and injection-locked DROs (IL-DROs) are used when the requisite frequency stability and phase noise cannot be achieved using stabilization techniques. A PL-DRO or IL-DRO approach also becomes necessary when multiple oscillators are required to be phase- or frequency-coherent, or both. For locked systems, a highly-stable, crystal-controlled signal source operating at high frequency (HF) or very high frequency (VHF) is used as a reference oscillator.

In injection (frequency)-locking, a VHF power amplifier driving a step-recovery diode generates a wide-band harmonic comb, which includes the required locking frequency. A bandpass filter selects the desired harmonic and a free-running DRO is locked to the harmonic through a phase-lock circuit (Fig. 2a).[3] ?

The main requirement in this case is to make sure that the DRO frequency drift under all ope conditions is less than th



3. Oscillator phase noise is characterized at some offset distance from the center frequency and normalized to a 1-Hz measurement bandwidth.



4. The phase noise of DROs based on bipolar transistors and GaAs MESFETs are compared at various frequencies.

locking bandwidth. This bandwidth is a function of the injection power, oscillator output power, and external Q. Injection-locking is simpler and less expensive than phase-locking, but the oscillator's RF output is more likely to contain spurious signals at the harmonics of the reference-oscillator frequency.

In a typical phase-locked DRO circuit (Fig. 2b), a DC-coupled sampler/phase detector mixes the desired harmonic of the amplified crystal oscillator with the incoming frequency from the DRO. If the difference frequency is small enough, the loop will be driven toward a point where the difference frequency out of the sampler becomes zero. The loop then drives the DRO toward a zero-phase-error condition.

A search mechanism is generally included in the system so that the loop will be forced to tune through a stable lock point if the initial difference frequency is too large for capture to occur. An AC-coupled phase-locked DRO circuit is used when the output frequency of the DRO is not harmonically related to the reference-oscillator frequency.

PHASE NOISE

Phase noise, related to short-term frequency stability, is characterized by variations in the output frequency which appear, in the frequency domain, as frequency-modulated (FM) energy around the carrier frequency (Fig. 3).

Phase noise is specified in levels relative to the carrier normalized to a 1-Hz bandwidth (dBc/Hz). It is measured at specified offsets from the carrier frequency: typical offsets are 10 and 100 kHz. In a DRO, phase noise is primarily dependent on the following factors:

- the low-frequency noise sources inherent in the active device designated by Sen(f), the noise spectral density at a frequency, f;
- the upconversion factor, F_c, a measure of the efficiency in the conversion of the low-frequency noise to the phase noise of the microwave oscillator;
- the loaded Q factor of the dielectric resonator; and
- the output power, P_o, and external Q of the oscillator.

The relation between the phase noise and these parameters is given by:

$$\Delta f_{eff} = F_c \, Sen(f) \times fm/(Q_{ext}) \, (P_o)^{1/2}$$

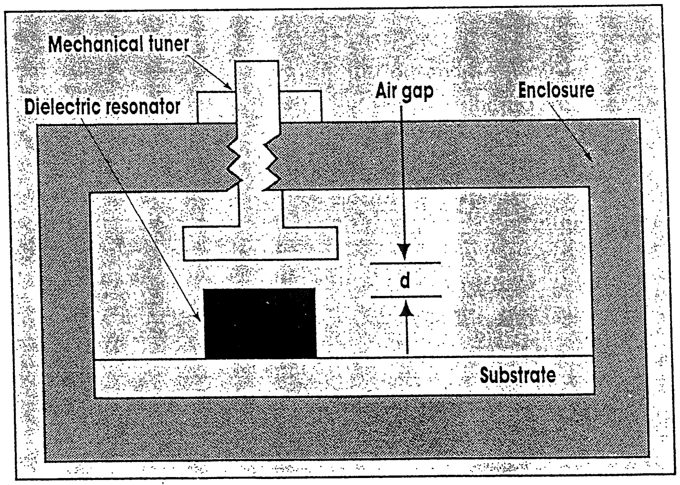
In this relation, Δf_{eff} represents the phase noise while fm is the offset frequency.

Optimization of phase-noise performance calls for the use of a high-Q dielectric resonator and a low-noise device combined with specific design considerations in the oscillator circuit. It has been proven that the low-frequency noise in a GaAs FET is inversely proportional to the gate length and width of the device. Both biasing conditions and the processing of the GaAs FET also play vital roles in achieving low-noise oscillators (Fig. 4).

Silicon bipolar DROs typically offer 6-to-10-dB improvement in the phase noise close to the carrier (to at least 100 kHz from the carrier) compared to FET versions. Fortunately, bipolar transistors are now available for use in fundamental-output oscillator circuits to frequencies as high as Ku-band.

Some of the newer design techniques that help further reduce phase noise include:

- Low-frequency feedback, using a parallel feedback circuit designed at frequencies to about 1MHz, can reduce upconversion of the low-frequency noise. Significant phase-noise improvement has been reported when using this technique.[4] This method is sometimes referred to as bias feedback.
- Noise degeneration, using the

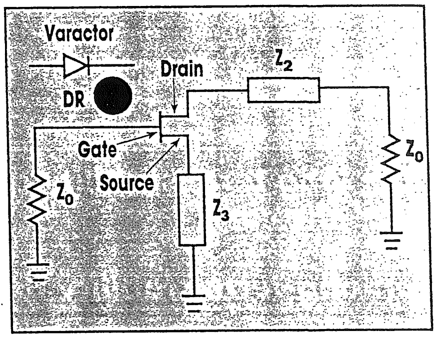


5. Mechanical DRO tuning is achieved with some form of screw mechanism that alters the oscillator's resonant cavity.

same dielectric resonator both as the frequency-determining element of the oscillator and the dispersive element of a frequency discriminator, can also cut noise. The DC output of the discriminator is applied to the frequency control port of the DRO. This technique has been reported to achieve phase noise as low as –120 dBc/Hz offset 10 kHz from a 10-GHz carrier.[5]

FREQUENCY TUNING

The frequency of oscillation of the dielectric resonator is dependent on a number of factors, not the least of which is its proximity to the ground plane. To take advantage of this, a tuning screw can be installed in the top cover directly above the resonator which, by reducing the distance between the resonator and the apparent ground plane, will provide for a certain amount of change in the resonant frequency (Fig. 5).

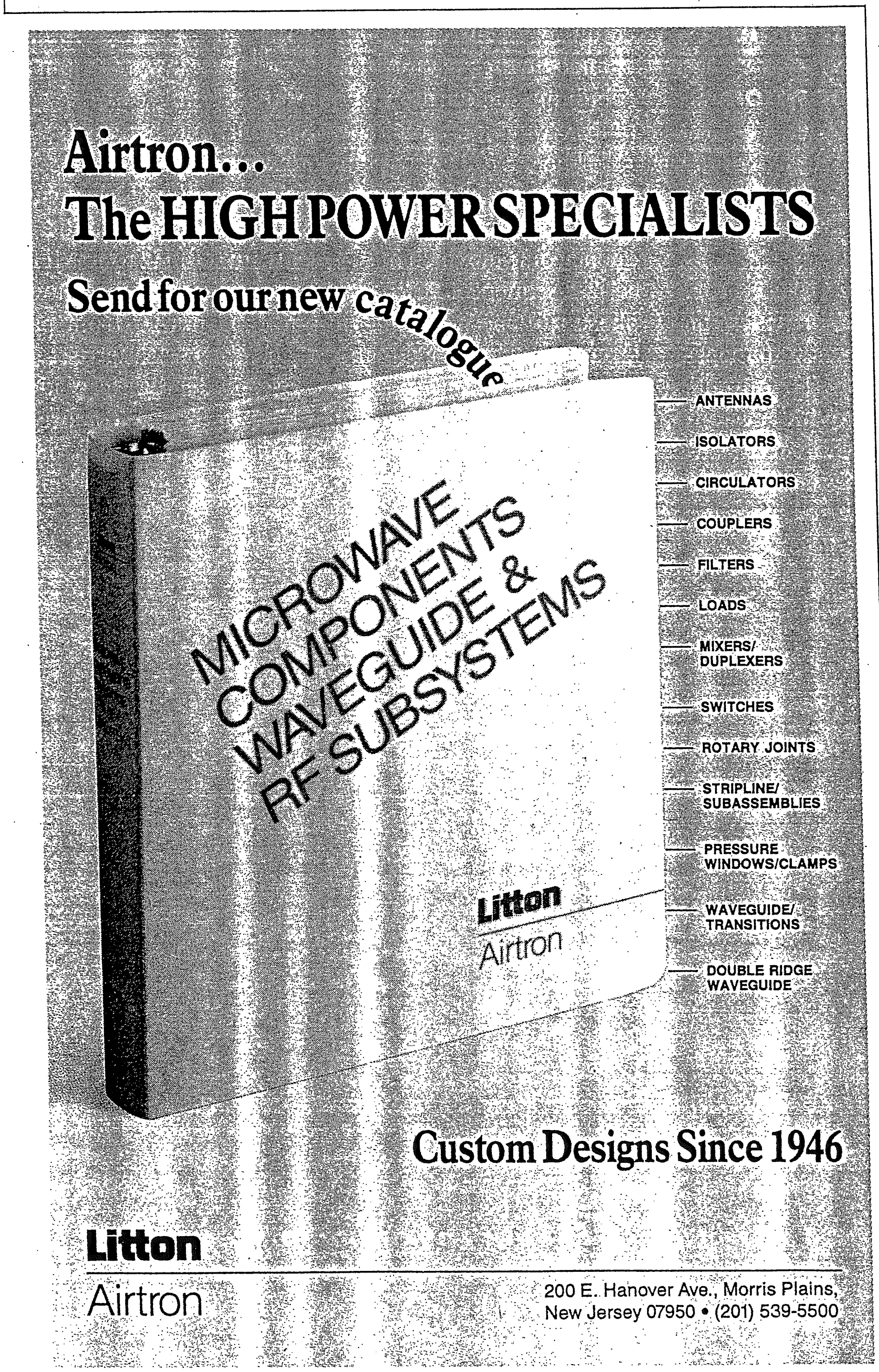


6. A typical scheme for electrically tuning a DRO employs a varactor diode to alter the capacitance at the resonator.

The reason for such behavior can be found in the cavity perturbation theory. Namely, when a metal wall of a resonant cavity is moved inward, the resonant frequency will decrease if the stored energy is predominantly in the electric field. Otherwise, when the stored energy close to the walls is mostly magnetic, as is the case for the shielded $TE_{01\delta}$ dielectric resonator, the resonant frequency will increase when the wall moves inward.

Current designs allow for up to 0.2-percent tuning range without significant degradation of other performance parameters. A properly-designed mechanical tuning option will provide a maximum tuning range while still maintaining hermeticity and reliability, and will not appreciably affect the resonator Q factor (apparent as a degradation in noise and power performance) or temperature stability.

Some applications, such as narrowband-modulated communication systems, FM-continuous-wave (CW) radar sources, or phase-locked-loop (PLL) systems, need electronic-tuning bandwidths on the order of 0.1 to 1.0 percent. These applications require sources with low phase noise,



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high tuning speed, and low tuning power. ET-DROs can now meet the rugged requirements for many such applications.

ET-DROs are also commonly used for analog or digital temperature compensation of the oscillator. This application requires that the frequency tuning range of the DRO exceeds the frequency drift of the oscillator under any combination of operating conditions (temperature, load, and bias variations). Various means can be used to electrically tune the DRO, including ferrite tuning, optical tuning, varactor tuning, and bias tuning.

Varactor tuning (Fig. 6) can provide up to 1-percent frequency adjustment. To permit varactor tuning, the dielectric resonator is coupled to another microstrip line connected to a varactor, resulting in mutually-coupled resonant circuits. The bias-voltage-dependent capacitance of the varactor varies the resonant frequency of the low-Q resonant circuit with the tuning voltage.

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The amount of frequency tuning is controlled by varying the coupling between the dielectric-resonator circuit and the microstrip line/varactor circuit.

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The amount of frequency tuning can be controlled by varying the coupling between the low-Q microstrip line/varactor circuit and the dielectric-resonator circuit. Tighter coupling permits greater tuning range. However, the attendant degradation in the Q factor manifests itself primarily as an increase in phase noise. Varactor tuning is by far the most common means of incorporating electronic tuning (Fig. 7). It should be noted that any increase in the electrical tuning range results in increased phase noise.

Bias-voltage tuning takes advantage of the frequency sensitivity to changes in the supply voltage of the oscillating device. By not using an internal voltage regulator, the oscillator can be designed to provide the necessary tuning range by varying the bias voltage, typically within 0.1

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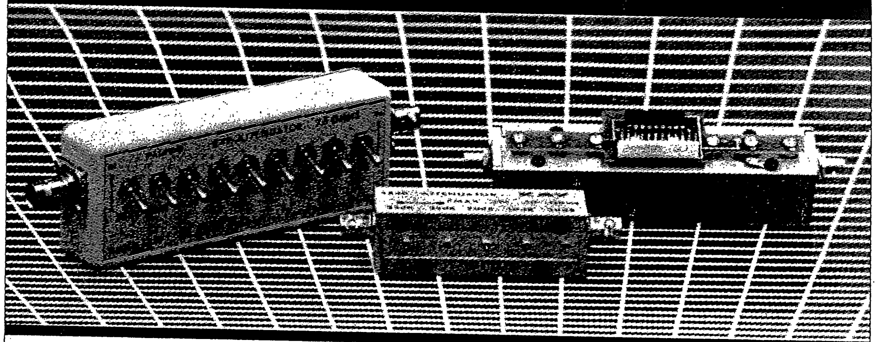

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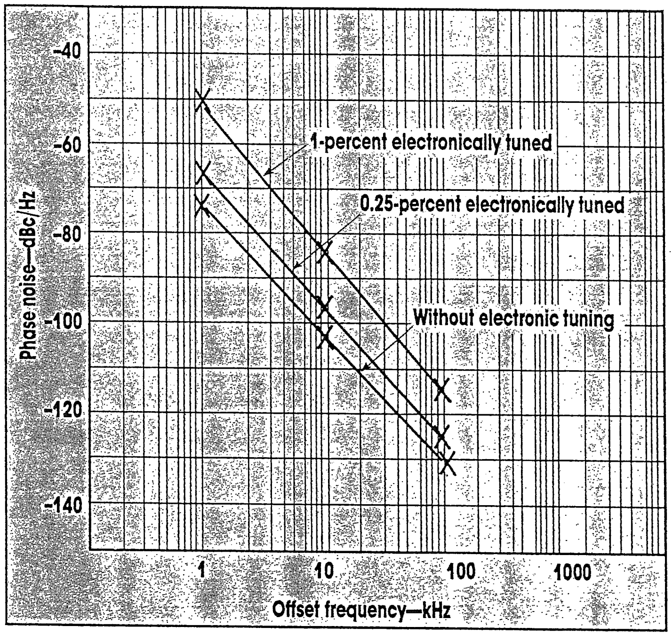
percent of the center frequency. This is sufficient frequency variation to compensate for the frequency drift of the oscillator over load and temperature variations, as well as the long-term drift due to component aging.

Better phase-noise performance can be achieved with the bias-tuned DRO than the varactor-tuned DRO. The latter requires the dielectric resonator to be simultaneously coupled to two microstrip lines, thus lowering the loaded Q factor of the resonator.[6] However, as the output power is often a function of the supply voltage, care must be exercised to maintain suitable output-power variation characteristics for the bias-tuned DRO.

DESIGN PROCEDURES

The minimum size of a practical DRO is primarily limited by the cavity required by the particular resonator. Normal design procedure calls for a separation of more than one resonator diameter between the resonator and its surrounding walls in order to properly excite the $TE_{01\delta}$ resonant mode. Also, the separation between the resonator and the housing lid should be of at least one resonator thickness to minimize the effects of the lid on the resonator performance. Too small a cavity can cause spurious-mode oscillation, as well as potentially causing Q-factor degradation.

Hermeticity is an important consideration when defining DRO requirements. Oscillators which are backfilled with a dry inert gas and then welded closed have less of a tendency to be susceptible to degradation due to long-term environmental effects. Hermetically-sealed oscillators are, of course, much more readily incorporated in a military system with the attendant performance and qualification requirements. Hermetic sealing is normally characterized by the helium leak rate of the DRO enclosure after it has seen a saturated helium environment. Typical leak rates of hermetically-sealed DROs are better than 10^{-7} cm^3 He/s.



7. These phase-noise characteristics were measured for various DRO tuning conditions at a center frequency of 10 GHz.

When a mechanical tuner is required, tuner construction, expected lifetime, over-travel protection, and ease of operation are also important considerations. A properly-designed mechanical tuner should provide the desired tuning range, be simple to adjust, have an acceptable number of operations, incorporate stops to limit travel, and still maintain case integrity and hermeticity.

Next month, this four-part series concludes with a review of some special DRO circuits. Notable among these designs are dual-resonator oscillators and selectable multiple-frequency oscillators. ••

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