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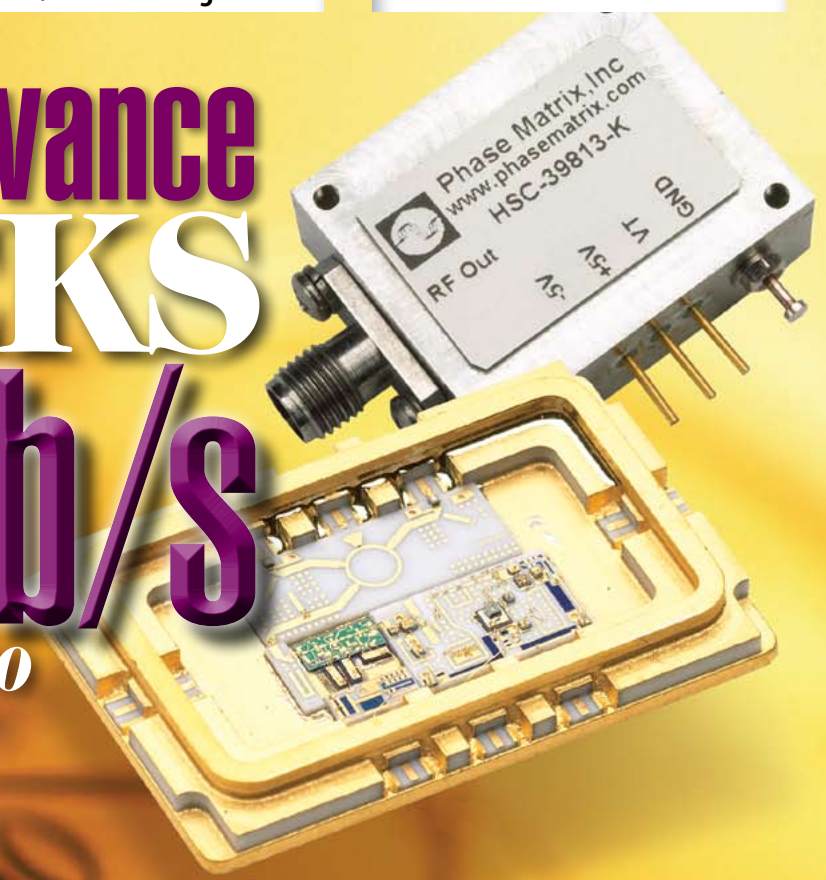

COVER story

Low-Jitter Modules Generate Clock Signals To 40 Gb/s

These low-jitter/low-phase-noise clock oscillator modules integrate silicon bipolar oscillators with frequency quadruplers to achieve stable output signals at 40 GHz.

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Billions of cellular telephones and their users worldwide are driving demands for faster communications networks. Optical communications systems support long-distance services and serve as the backhaul communications for wireless networks. At one time, optical communications systems operating at 10 Gb/s (OC-192) may have seemed adequate but, with growing voice, data, and video traffic, optical communications networks carrying data rates of 40 Gb/s (OC-768/STM-256) are becoming more commonplace. Beyond that, several companies have already demonstrated components for systems operating to 160 Gb/s.

1. Model HSC-41415-08K is a low-jitter, wideband clock oscillator that provides tunable single-ended output signals from 39.81 to 43.01 GHz via a coaxial K connector. [Photo of HSC-41415-08K]

For example, at the 2007 Optical Fiber Conference, IBM (www.ibm.com) researchers detailed a prototype optical transceiver chipset capable of 160 Gb/s speeds[1]. The optical transceiver technology is based on CMOS process technology and can be integrated with other optical components fabricated on indium phosphide (InP) and GaAs into a common module that can easily mount onto a high-speed printed-circuit board (PCBs) for use in a wide range of systems and products.

Prior to that, in March 2006, Oki Electric Industry Co., Ltd. (www.oki.com) reported on the successful transmission and reception of 160 Gb/s data over a distance of 635 km. The experiment was part of the "Research and Development on Ultrahigh-speed Backbone Photonic Network Technologies" project consigned by Japan's National Institute of Information and Communications Technology (NICT). The data transmission included high-speed video.

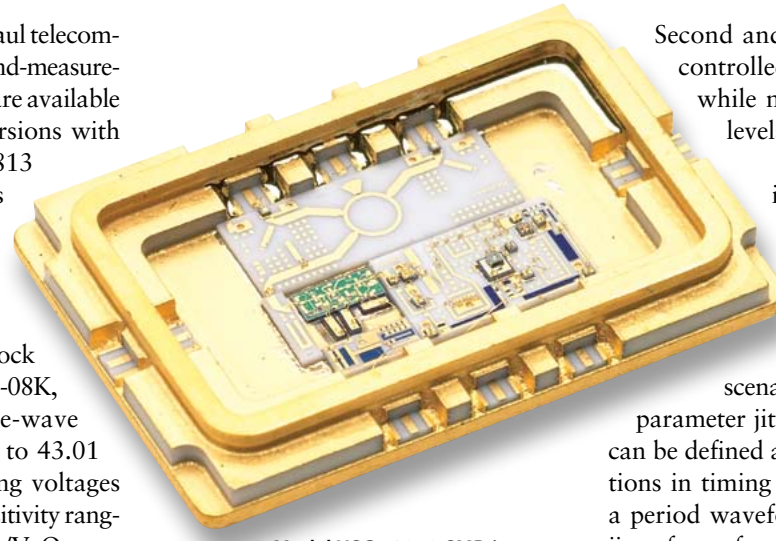
For all of these high-speed networks, the system clock is one of the more critical components, and Phase Matrix (San Jose, CA) is addressing that need with high-performance, low-jitter clock

modules suitable for long-haul telecommunications as well as test-and-measurement applications. Models are available in coaxial single-ended versions with sine-wave outputs from 39.813 to 43.018 GHz as well as in compact surface-mount housings with differential-output sine wave signals at 39.813 and 43.018 GHz.

The coaxial 40-Gb/s clock oscillator, model HSC-41415-08K, provides single-ended sine-wave output signals from 39.81 to 43.01 GHz controlled by a tuning voltages of 0 to 12 V with tuning sensitivity ranging from 300 to 600 MHz/V. Output signals are at +5 dBm or more, available at a K connector. Ideal for OC-768/STM-256 applications, the low-jitter clock oscillator features a fast slew rate of 25 V/ns or better, 50-percent typical duty cycle, and minimum modulation bandwidth of 20 MHz.

Model HSC-41415-08K consists of a 10-GHz low-noise silicon-bipolar transistor oscillator with tuning by means of a hyper-abrupt silicon varactor diode. The silicon bipolar transistor features a maximum frequency of oscillation (f_{max}) of 40 GHz and maximum available gain of 16 dB at 4 GHz. The device features a common-collector configuration and uses 40 emitters with emitter width of 0.5µm and 2-µm emitter-to-emitter width. The oscillators feature a planar microstrip resonator with optimized quality factor (Q) for low noise at 10 GHz.

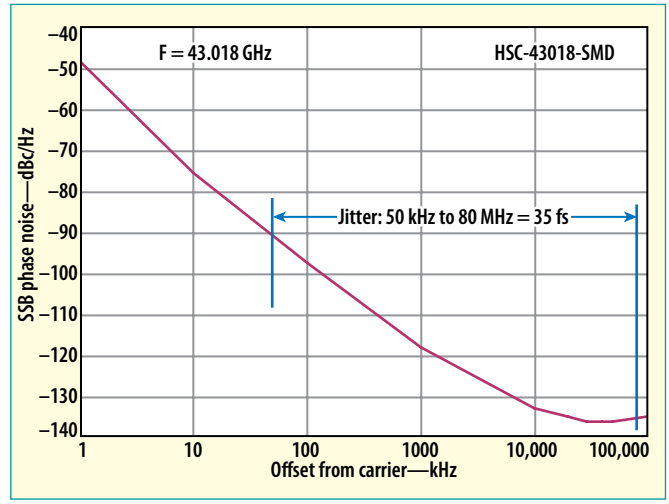
The varactor diode provides enough tuning range to compensate for aging effects or frequency variations due to temperature. Within model HSC-41415-08K's package, 10-GHz signals are multiplied to 40 GHz by means of a GaAs pseudomorphic-high-electron-mobility-transistor (PHEMT) frequency multiplier. The outputs of the multiplier are boosted and buffered by means of a low-noise GaAs



2. Model HSC-43018-SMD is a low-noise, surface-mount clock oscillator that provides differential sine-wave output signals centered at 43.018 GHz with enough tuning range to overcome temperature drift and aging effects and for phase-lock applications.

FET monolithic-microwave-integrated-circuit (MMIC) amplifier. Prior to the output connector, signals are passed through a bandpass filter to minimize harmonic and subharmonic feedthrough signals.

The approach results in phase noise of typically -90 dBc/Hz offset 100 kHz from the carrier and -130 dBc/Hz or better 10 MHz from the carrier.



3. The phase noise of the HSC-43018-SMD surface-mount clock oscillator is better than -95 dBc/Hz offset 100 kHz from the carrier.

Second and third harmonics are controlled to typically -30 dBc while nonharmonic spurious levels are typically -30 dBc.

Phase noise, of course, is commonly used to characterize oscillator quality in analog or frequency-domain systems. But in digital or time-domain scenarios, the closely related parameter jitter is often used. Jitter can be defined as the unwanted variations in timing over some portion of a period waveform with respect to a jitter-free reference. It can be specified in terms of phase units, such as radians, time units, such as seconds, or unit intervals (UIs). Because jitter is difficult to measure directly, especially at rates as high as 40 Gb/s, it is often calculated from measurements of integrated phase noise performed with a phase-noise test system for a given expanse of fixed offset bandwidths, such as 50 kHz to 80 MHz for OC-768 systems.

Phase noise at offset frequencies close to the carrier plays a much larger role in the effects of the integrated phase noise (jitter). Phase noise at frequencies far from the carrier (10 MHz and greater) has little effect on jitter, whereas phase noise close to the carrier (50 kHz to 1 MHz) has significant effects on jitter performance. For the model HSC-41415-08K clock oscillator, the maximum jitter is only 200 fs for offsets from 50 kHz to 80 MHz. (For those seeking to better understand jitter, Phase Matrix offers a phase-noise-to-jitter conversion tool at its web site, at http://www.phasematrix.com/design_tools/Jitter.html).

The wide tuning range of the model HSC-41415-08K is more than adequate to correct for frequency drift in typical single-frequency OC-768 applications, since maximum frequency drift with temperature is 100 MHz. Frequency

pulling for a 12-dB return-loss load is a maximum of 10 MHz while frequency pushing is a maximum of 20 MHz for power-supply variations of +/-0.2 VDC. The model HSC-41415-08K clock oscillator is supplied in a machined aluminum housing measuring 1.18 x 0.95 x 0.5 in. It requires supply voltages of +6 and - 6 VDC and is rated for operating temperatures from 0 to +70 °C.

For applications requiring differential sine-wave signals, models HSC-39813-SMD and HSC-43018-SMD from Phase Matrix provide outputs centered at 39.813 and 43.018 GHz, respectively, with modulation bandwidth of at least 100 MHz. Output levels are at least 0 dBm or 0.6 V peak to peak at each differential port. Unlike the HSC-41415--08K, which can tune across the full range from 39.813 to 43.018 GHz, these smaller surface-mount clock oscillators provide moderate tuning ranges around 39.813 or 43.018 GHz. Tuning voltages of 0 to 5 V provide tuning sensitivity of 40 to 80 MHz/V. The low-jitter oscillators achieve a fast slew rate of 25 V/ns or better and operate with typical 50-percent duty cycle,

As with the HSC-41415-08K, these surface-mount clock oscillators feature excellent phase-noise performance even at these millimeter-wave frequencies, with phase noise of better than -95 dBc/Hz offset 100 kHz from the carrier and better than -130 dBc/Hz offset 10 MHz from the carrier. In terms of the time domain, the maximum jitter is 100 fs. Second- and third-harmonic levels are typically -30 dBc while nonharmonic spurious levels are typically -30 dBc. Frequency drift with temperature is 100 MHz or less while frequency pulling for a 12-dB-return-loss load is 100 MHz. Frequency pushing is 20 MHz or less for +/-0.2-V supply variations. The HSC-39813-SMD and HSC-43018--SMD clock oscillators operate with positive and negative supply voltages of +6 and -6 VDC. They are each supplied in a miniature surface-mount package measuring 0.679 x 0.447 x 0.17 in

Low jitter clocks are key parts of all high-speed optical communications used both for backbone transport or metropolitan-area/enterprise solutions. Such clocks are also vital for the test and measurement set-ups for the high-speed systems. The new high-speed clocks from Phase Matrix are suitable for long-haul applications as well as in test-and-measurement equipment. The company's sources are available in single-ended and differential formats for use in commonly used forward-error-correction (FEC) systems at 39.813 and 43.018 GHz. The high-frequency clocks can be readily phase-locked for stability, and

are also available to support high-speed systems requiring half-rate clocks (19.906 and 21.509 GHz). In addition, the company offers low-jitter clock oscillators with similar characteristics at 25 and 50 GHz in support of higher-speed 100-Gb/s optical communications systems.

For those working at lower frequencies, for example, the company offers several very compact solutions as clock sources, including the tiny pin-packaged model FTO-2488-TD with fixed 2.488-GHz differential sinewave output. Measuring just 0.18 in. high by 0.5 in. in diameter, the miniature, hermetically sealed clock oscillator is ideal for transmitter data retiming and for receiver data recovery applications in more modest-frequency systems. It incorporates a silicon bipolar buffer amplifier to achieve 0 dBm output levels at each differential port with extremely low jitter of less than 50 fs when measured from 50 kHz to 80 MHz from the carrier frequency.

Model FTO-2488-TD is based on a low-noise silicon bipolar active device and achieves typical phase noise of -108 dBc/Hz offset 100 kHz from the carrier. Second-harmonic levels are at least -20 dBc below the carrier while third-harmonic levels are -20 dBc or better. The tiny clock source draws a maximum of 100 mA current from a typical +3.3-VDC supply.

In addition, the model HSC-2000-FD and HSC-2500-FD provide fixed differential outputs of 2.0 or 2.5 GHz with worst-case stability of 50 PPM over the full operating-temperature range and at least 0 dBm output power at each differential port. Supplied in a flatpack housing measuring just 2.5 x 1.5 x 0.35 in., the high-stability, hermetically sealed clock oscillators achieve low phase noise of better than -125 dBc/Hz offset 10 kHz from the carrier., with performance of -130 dBc/Hz offset 100 kHz from the carrier and -150 dBc/Hz offset 100 MHz from the carrier. As with the other Phase Matrix clock oscillators, they are designed for low power consumption, typically drawing 250 mA current from a +5-VDC supply. Spurious levels are typically only -60 dBc. The low-noise clocks exhibit second-harmonic levels of -15 dBc or better and third-harmonic levels of -20 dBc or better. **Phase Matrix, Inc., 109 Bonaventura Dr., San Jose, CA 95134-2106; (408) 428-1000, e-mail: sales@phasematrix.com, Internet: www.phasematrix.com.**

REFERENCE

1. C. L. Schow, F. E. Doany, O. Liboiron-Ladouceur, C. Baks, D. M. Kuchta, L. Schares, R. John, and J. A. Kash, "160-Gb/s, 16-Channel Full-Duplex, Single-Chip CMOS Optical Transceiver," 2007 Optical Fiber Conference, March 29, 2007, Anaheim, CA.