A 4 GHz DRO

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Introduction

This paper describes the design of a 4 GHz dielectric resonator stabilized oscillator using the Avantek AT41400 silicon bipolar transistor chip. The design is done on a personal computer using Touchstone and Microwave Spice, both from EEsof. The oscillator is then constructed, and its performance is measured. The result is an oscillator with exceptional phase noise performance.

Design

An oscillator design flow chart is shown in Table 1. The first step in the design is to acquire the device S-parameters at the bias to be used. To do this, a simulation of the chip was run on microwave Spice using an equivalent circuit model from the device design cycle. The resulting S-parameter file can be used directly in Touchstone for the design. A bias point of V_{CE} = 7.5 V and I_{CE} = 30 mA is used for this design.

A common base topology with L_B = 0.5 nH is selected as a starting point. This should ensure k<1 for the device. The circuit is then simulated on Touchstone, with a 1K resistor used as a simplified dielectric resonator model. The resulting file is given in Figure 1. The procedure used is to first verify k<1, then tune l and L_B (Figure 2) for $|S_{22}| > 100$, which ensures oscillation into a 50 Ω load or $|S_{22}|\,\Gamma_L = 1$.[1] The resulting optimized schematic diagram is shown in Figure 2b.

Fabrication and Test

The oscillator uses a Transtech D8500 resonator with ϵ_r = 38, D = .620" and h = .248". The temperature variation of the oscillator is 3.8 ppm/°C over a temperature

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CKT
! AT41400 AT 7.5V,30MA AS DSO
! SETUP FOR CB OPERATION WITH INPUT RESONATOR

  S2PA    3   2   1      AT414CE.S2P        !CE S PAR CONNECTED CB
  IND     3   0          L\.5                   !LB
  DEF2P   1   2          XR

  IND     4   1          L=.5               !LE
  TLINP   4   5          Z=50 L\225 K=6.6 A=0 F=1
  RES     5   6          R=1000
  CAP     5   6          C=40
  IND     5   6          L=.04
  TLINP   6   7          Z=50 L=250 K=6.6 A=0 F=1
  XR      1   2
  DEF2P   7   2          OSC

FREQ
  STEP   4

OUT
  OSC     S22
  XR      K

OPT
  OSC     MAG[S22]>100
```

Fig. 1 Touchstone circuit simulation printout.

TABLE I

OSCILLATOR DESIGN FLOW CHART
SELECT DC BIAS
↓
GENERATE S-PARAMETERS FROM MICROWAVE SPICE OR DATA SHEET
↓
TOUCHSTONE TWO-PORT OSCILLATOR DESIGN
↓
BUILD PHYSICAL OSCILLATOR

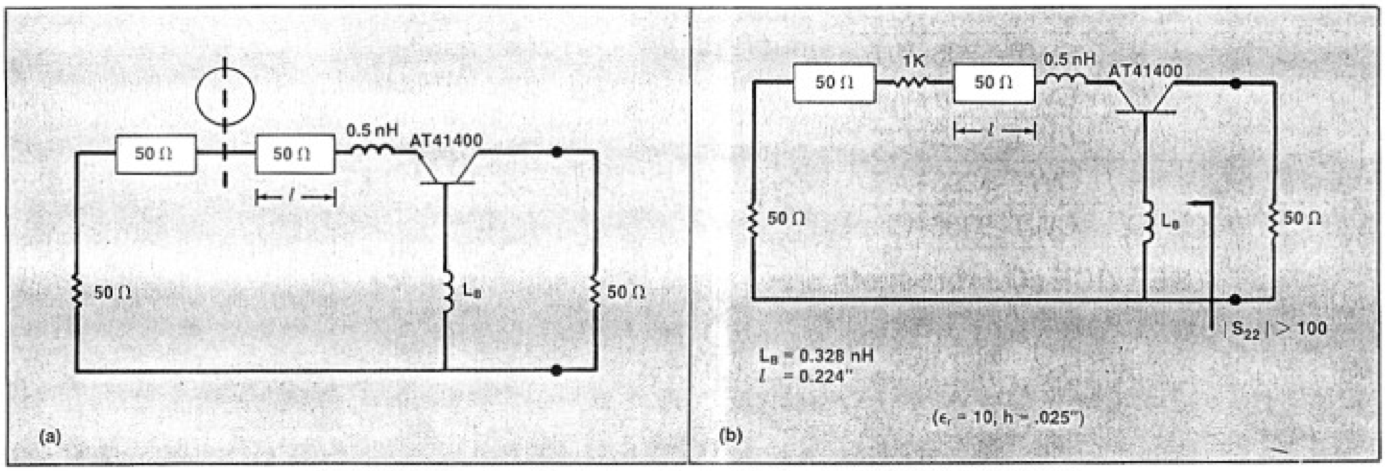


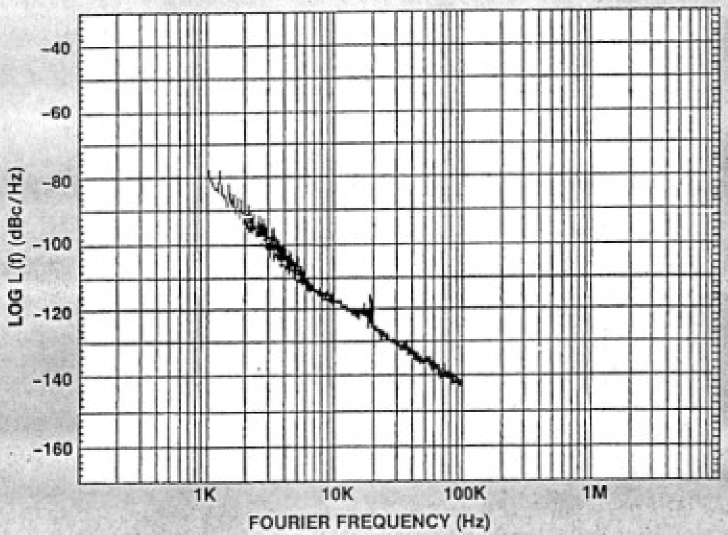
Fig. 2 (a) DRO schematic diagram; (b) simplified model with DR at resonance.

range of −54 to +85°C. The selection and coupling of the resonator is described in reference 2.

The external Q of the oscillator was found to be 5800 at 4.0 GHz. The RF output power was 14.2 dBm at V_{CE} = 7.5 V, I_{CE} = 30 mA. The harmonics were:

$$F2 = -22 \text{ dBc}$$
$$F3 = -26 \text{ dBc}.$$

The phase noise of the oscillator is given in Figure 3, which shows L = −117 dBc/Hz at 10 kHz offset from the carrier, an excellent result. ■



TEST FREQUENCY = 4006 MHz

OFFSET FROM CARRIER (kHz)	L (dBc/Hz)
1.0	−76.64
2.0	−87.64
5.0	−106.04
10.0	−117.09
20.0	−125.20
50.0	−136.75
100.0	−143.80

Fig. 3 Normalized phase noise SSB power spectral density.

References

1. Vendelin, G.D., *Design of Amplifiers and Oscillators by the S-Parameter Method*, John Wiley, 1982, Chapter 4.
2. Kajfez, D., P. Guillon, *Dielectric Resonators*, Artech, 1986, Chapter 10.

Avantek/EEsof will be presenting an applications seminar giving more details on this design technique beginning in July. More information about the seminar is available from:

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