Ultra-Broadband Contiguous Planar DC-35-65 GHz Diplexer using Softboard Suspended Stripline Technology

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***Abstract* --- This article describes a novel phase linear, sharp & symmetrical roll-off, ultra- wideband, contiguous, planar diplexer using Suspended Stripline (SSL) technology implemented on RO5880 dielectric material. The lowpass and highpass channels cover wide bandwidth of DC-35GHz and 35GHz-65GHz respectively. The synthesis, design and simulation of the diplexer is done using closed form analytical model in AWR's iFilter. Final design of the diplexer is optimized using CST a 3D EM simulator.**

***Index Terms* – Suspended Stripline, contiguous diplexer, soft-board, recessed cavity, lowpass filter, highpass filter, millimeter wave diplexer.**

I. INTRODUCTION

Diplexers are key components employed in the front-ends of MW or MMW broadband signal acquisition and processing systems. Applications of diplexers include EW Systems, Communication Systems as well as Test instruments. The wideband diplexer presented in this paper was designed to support the front end of a new test equipment covering frequencies up to 65 GHz. Diplexers at mmw frequencies up to V band have been reported before using fused silica and alumina [1]. These diplexers not only represented higher losses but also lacked symmetrical and sharp roll-off required by many applications.

This paper represents a wideband contiguous SSL diplexer that includes lowpass and highpass filter substrate suspended symmetrically between two ground planes. SSL has some attractive features compared to conventional microstrip and stripline, including better temperature stability, less dispersion, flatter group delay, and low-loss over wider frequency bandwidth. The planar substrate used is RO5880 material with dielectric constant of 2.1, and effective dielectric constant is closer to 1 due to SSL structure.

Fig. 1 shows a contiguous diplexer, realized by paralleling a lowpass filter (LPF) and a highpass filter (HPF) at a common junction.

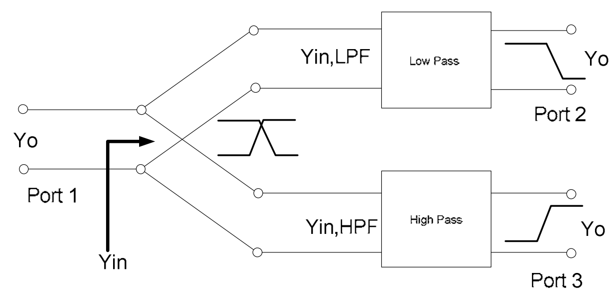

Fig. 1. Equivalent Circuit of a contiguous Diplexer

In order to obtain matched input port, the complex input admittances $Y_{in,LP}$ and $Y_{in,HP}$ of the two filters should satisfy the equation below over the frequency band [1]:

$$Y_{in} = Y_{in,LP} + Y_{in,HP} = Y_0 \qquad (1)$$

This condition can be represented by real and imaginary parts [1]:

$$\mathrm{Re}(Y_{in,LPF}) + \mathrm{Re}(Y_{in,HPF}) = Y_0 \qquad (2)$$

$$\mathrm{Im}(Y_{in,LPF}) + \mathrm{Im}(Y_{in,HPF}) = 0 \qquad (3)$$

Two singly terminated Tchebyshev complementary filters which satisfy above conditions are used to realize this high performance diplexer. A closed form lumped element simulation of a contiguous diplexer with a crossover frequency fc of 35 GHz was performed using AWR's Microwave Office.

The lowpass filter and highpass filters of the diplexer are implemented based on 13 section and 11 section Tchebyshev design respectively. These filters are implemented on a 5 mil soft substrate housed in a proportionally recessed cavity of suspended stripline structure.

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The height and the width of the recessed cavity that forms a waveguide channel and strip width are optimized such that the first higher order modes are moved out of the frequencies of interest [2]. The cavity channel width ‘a’ and suspended strip width are selected to avoid higher order mode propagation and to ensure that the propagation mode is TEM [3]. The suspended stripline operating frequency range or cutoff frequency is given in equation below

$$f_c = c/2a \qquad (4)$$

Where c is the speed of light and a is the channel width.

II. Filter Design

A. Diplexer model and synthesis

The initial synthesis of the lowpass and the highpass filter of the diplexer model is completed using closed form admittance inverter equations that require parameters of Tchebyschev low-pass prototype in conjunction with AWR’s Microwave Office simulation [3], [4].

B. Lowpass Filter

The Tchebyschev lowpass section of the diplexer is modeled and synthesized using iFilter feature in AWR. The lowpass 13th order stepped impedance design is implemented using series $\lambda/8$ high impedance and shunt $\lambda/2$ low impedance resonators. The cutoff frequency of the filter is set to 35GHz with pass-band ripple of 0.1dB.

C. Highpass Filter

The LC lumped element prototype circuit of the Tchebyshev 11th order highpass is synthesized using iFilter feature in AWR for the corner frequency at 35 GHz.

The series capacitances of the high-pass are implemented using broadside coupled strip elements on either side of the substrate. The shunt inductances are implemented using short circuited step impedance line resonators with nominal electrical length of $\lambda/2$ [3], [5].

Physical lengths of the resonators and overlap sections of highpass filter are finely optimized in CST for the required performance.

D. Simulation

The diplexer design specifications are shown in the table below

Table 1
Design Specifications

Parameter	Attenuation (dB)	Frequency range (GHz)
$\lvert S_{11}\rvert$	≤ -12	DC-65GHz
$\lvert S_{22}\rvert$	≥ -12	DC-35GHz
$\lvert S_{33}\rvert$	≥ -12	35-65 GHz
$\lvert S_{21}\rvert$	≤ -1	DC-35 GHz
$\lvert S_{31}\rvert$	≤ -2	35-65 GHz
$\lvert S_{21}\rvert$	≤ -5	At cross-over

In terms of design perspective of the diplexer, the layout of the synthesized LPF and HPF filter is transferred to 3D EM software (CST) and optimized for required parametric performance. The 3D EM simulation and optimization was done using CST’s Transient Solver by exciting Gaussian waveform at all three ports of the diplexer. Enhanced accuracy of 40 dB was used representing 99% decay of the energy in the electromagnetic structure. Finite integration method in conjunction with perfect boundary approximation was used. Mesh line ratio limit of 35 was implemented with 15 lines per wavelength at the highest frequency of operation [6].

Electric field patterns for the optimized design at the lowpass, highpass and crossover point are shown in figures 2, 3 and 4 below respectively.

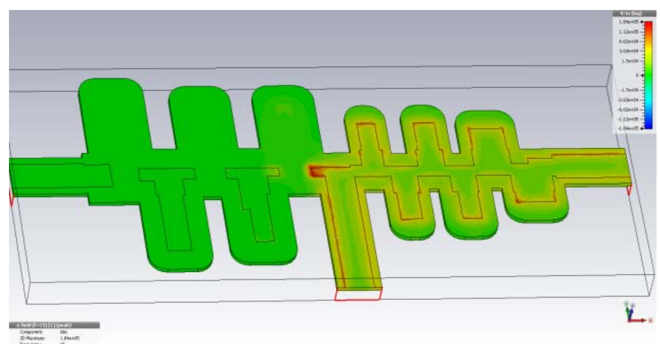

Fig. 2. Simulated E-Field at 15 GHz (LP Frequency)

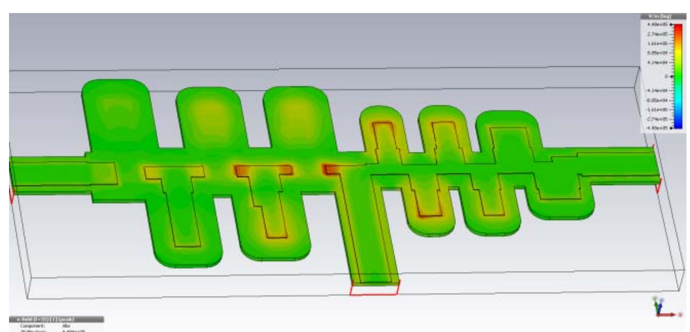

Fig. 3. Simulated E-Field at 35 GHz (Cross Over)

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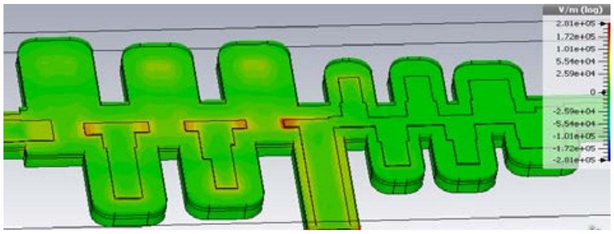

Fig. 4. Simulated E-Field at 50 GHz (HP Frequency)

The simulated log magnitudes of the S-parameters of the optimized diplexer are shown in figure 5 below:

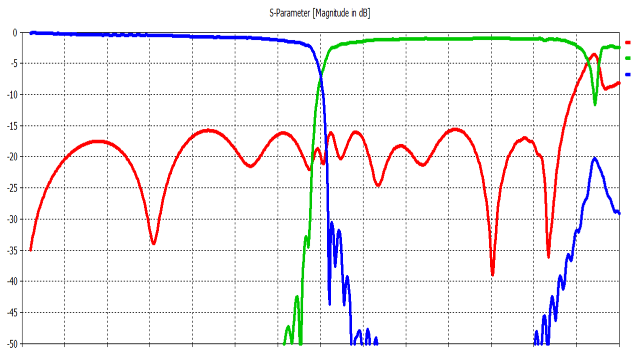

Fig. 5. Diplexer Simulated Response from DC to 70 GHz

E. Fabrication

Gold plated brass was used for the mechanical housing and recessed cavities. High frequencies demand higher accuracy of the mechanical cavity as well as etching of the PCB. Mechanical machining accuracies better than 0.2 mils and PCB etch tolerance of better than 0.5 mils were held in order to achieve a good co-relation between simulated and the measured results. Provision for tuning screws as shown in Fig. 6 below was kept to make any minor changes in the measured response. Four hole flange 1.85 mm connectors were implemented on all three ports.

Fig.6. Wideband DC-35-65 GHz Diplexer final assembled.

Fig. 7 shows fabricated PCB laid flat on the bottom part of the diplexer housing. The guided dowel pins provide accurate and symmetrical positioning of the strip width in the waveguide channel.

There are five mounting screws that clamp the top and bottom parts of the housing with PCB sandwiched in between. The two parts of the metal housing come in close contact with the copper thru plated via holes on the PCB. The diameter and position of ground via holes are optimized to provide improved grounding at higher frequencies

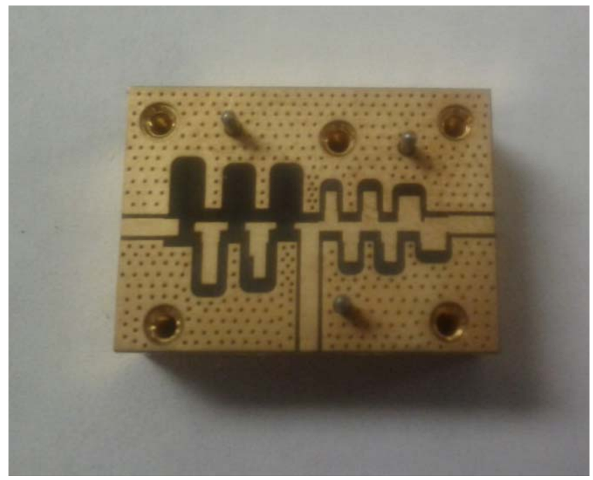

Fig.7. Diplexer suspended substrate

III. Measured Results

Results were measured using Agilent 70GHz VNA. The VNA was calibrated using well-defined short, open, and 50 ohm load 1.85 mm standards. Through (Thru) connection was formed by connecting the two reference planes together to complete the SOLT (Short, Open, Load, and Thru) calibration.

Fig. 8 represents measured results of diplexer response. Excellent co-relation between the simulation and the measured results was observed as apparent from Fig 5 and Fig 8. This diplexer provides less than 0.5 dB ripple and 1.3dB loss at the highest frequency of the passband (65GHz) and a loss of 5 dB at the crossover point. 20 dB roll-off point on LPF and HPF is less than 1 GHz away from the crossover point.

Overall return loss was measured to be better than 12 dB. Excellent phase response linearity on HP and LP side was achieved around the cross over point.

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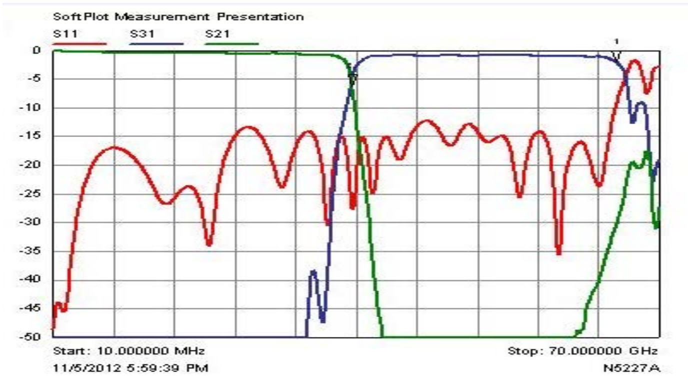

Fig. 8. Diplexer Measured Response from 10 MHz to 70 GHz

IV. CONCLUSION

A novel high performance planar contiguous diplexer is presented covering DC-35-65 GHz. Excellent flatness and roll-off sharpness are achieved. Return loss better than 12 dB was measured across the band. Excellent correlation between measured and simulated results were achieved with minimal post tuning.

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