Low Jitter Silicon Bipolar Based VCOs for Applications in High Speed Optical Communication Systems

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***Abstract* — This paper describes the design of silicon bipolar-based planar microstrip low noise VCO at 10GHz. Using this VCO with GaAs PHEMT MMIC frequency multipliers, 20GHz and 40GHz VCOs are reported. Applications include OC-192 and OC-768 optical communication systems. Demonstrated phase noise of -113 dBc/Hz@100 KHz represents the best phase noise of a 10GHz microstrip VCO reported to date.**

I. INTRODUCTION

The fast growing high-speed infrastructure market has created huge demand for high performance high frequency components. In the recent WDM systems bit rate up to 10Gb/s per channel has already been used and systems with 40Gb/s bit rate are now in development. High frequency components based on microwave technology are needed for use in in the 10Gb/s (OC-192 and STM-64) and 40Gb/s (OC-768 and STM-256) transmitter and receiver sub-systems as shown in figure 1 and 2. Low jitter VCO is a key component for the data retiming in the transmitter subsystem and clock and data recovery in the receiver system.

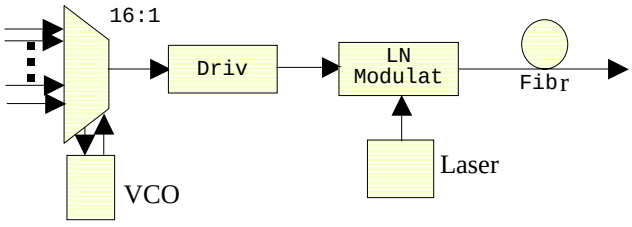

Fig.1 Transmitter Block Diagram of Optical Comm. System

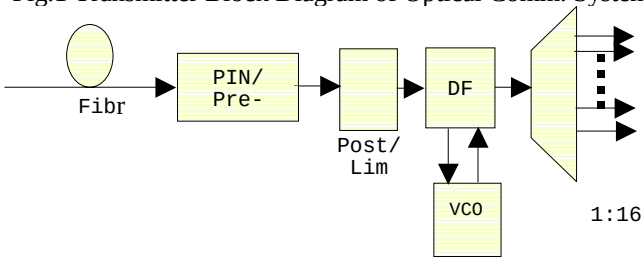

Fig.2 Receiver Block Diagram of Optical Comm. System

At speeds 10Gb/s and above hybrid VCOs have a unique performance advantage over the integrated IC solutions. These speeds place stringent demands on the performance characteristics of the VCOs in terms of jitter, modulation bandwidth and linearity. At higher speeds reduced Quality factor of the on-chip resonator combined with the higher 1/f noise of the high speed integrated devices limit the performance of the on chip VCOs.

This paper describes a new hybrid VCO using a low noise silicon bipolar transistor at 10GHz, which combined with frequency multiplier MMICs, is capable of generating very low noise signals at 10, 20 or 40 GHz. Various options have been described and comparisons for generating low jitter sources at 10, 20 and 40GHz are presented. A new solution for planar low jitter sources using mature technology components is presented.

II. JITTER AND PHASE NOISE

Jitter and phase noise are closely related. In the digital world the quality of the signal source is measured in the form of Jitter. Low jitter clock source is a key requirement of a communication system. Clock jitter is defined as the variation in timing of a critical instant in a periodic waveform with respect to a jitter free reference. Jitter in a system has three different forms: Jitter Transfer, Jitter Tolerance and Jitter Generation. In interpreting the clock sources it is the Jitter generation, which characterizes the clock. At lower speeds high speed oscilloscopes or communication analyzers can easily measure the jitter from the wave shape. However at 10Gb/s and above it is much harder to measure the clock jitter using classical methods.

Phase noise measurement capable of measuring extremely low-level instabilities is a practical tool to interpret the source jitter. Jitter is calculated from the measurement of integrated phase noise over a fixed offset bandwidth (50KHz to 80MHz for OC-192 for example) and is represented in many units including: radians, degrees, time (secs.) and UI (unit interval). Phase noise at the close-in

frequencies plays a much larger role than the phase noise at frequencies far from the carrier. It can be shown that the effect of phase noise at offset frequencies beyond 10 MHz has negligible effect on the integrated phase noise over 50KHz to 80 MHz. Phase noise from 50 KHz to 1 MHz on the other hand plays significant role on the jitter performance.

III. OPTIONS FOR HIGH FREQUENCY SOURCES

A number of options exist to generate low noise oscillators at microwave and millimeter wave frequencies. Each of these options has its unique features. At speeds lower than 10Gb/s VCO function has already been integrated on the Mux/Demux ICs. At speeds of 10Gb/s and above, hybrid VCOs are preferred particularly for long-haul applications due to significantly better jitter performance. We will briefly look at some of the commonly usable approaches of hybrid VCOs. There are two basic options for signal generation at microwave/millimeter wave frequencies: Fundamental Oscillator and Frequency Multiplied Oscillator.

Fundamental Oscillators:

Using GaAs FET / PHEMT devices fundamental oscillations at 40 GHz can be easily obtained. These devices however are inherently noisier than Silicon devices. Silicon bipolar devices however are limited in high frequency performance to less than 20 GHz. Fundamental Silicon bipolar VCOs can be effectively used for OC-192 applications. SiGe device technology is an emerging technology and has recently been shown to have potential for low phase noise fundamental mmw sources [1]. Dielectric resonator FET oscillators and YIG tuned FET oscillators are known to provide low noise fundamental oscillations. The phase noise for a DRO has been reported to be –104 dBc/Hz at 36 GHz [2] and –100 dBc/Hz at 100KHz for a 20-40GHz YIG tuned oscillator [3]. These oscillators however represent large size, higher cost and potential sensitivity to microphonics compared to microstrip VCOs. YIG oscillators additionally require significantly larger dc power consumption.

Frequency Multiplied Sources:

In order to achieve low jitter hybrid signals sources for 40Gb/s systems, frequency multiplied sources can be used effectively. A low noise silicon bipolar oscillator followed a GaAs PHEMT MMIC frequency multiplier is a simple and cost effective configuration for generating 20 GHz and 40 GHz signals required for OC-768 and STM-256 systems.

Frequency Multiplied oscillators represent an advantage in achieving a lower phase noise at the cost of sub-harmonically related spurious. Lower phase noise devices coupled with higher Q resonator provide a lower phase noise source. The undesired spurious at sub-harmonically related frequencies is solved by providing proper filtering in the output.

Low Noise Techniques:

A number of factors need to be optimized for low noise signal generation.

a) Low noise device is an important requirement to start with. Silicon Bipolar transistors have 1/f corner frequency of less than 10 KHz making it the most commonly used device for low noise oscillators. In this oscillator low phase noise performance is enhanced due to low density of surface states between base and the emitter caused by proprietary passivation techniques. However the high frequency operation of these devices is limited to less than 20GHz[4].

b) Quality factor of the resonating element is another factor in the determination of low phase noise. In this design a high Q microstrip resonator has been used. Quality factor of the resonating element is a function of its physical parameters, which were optimized to achieve highest practical Quality factor. Q of greater than 50 was achieved.

c) Circuit design optimization also plays a critical role in the low phase noise oscillators. The condition of perpendicularity between device line and the load line at the intersection point at the frequency of operation is important to achieve best phase noise.

IV. DEVICES AND DESIGN

The oscillator uses an Agilent S240 low noise Silicon Bipolar transistor (figure 3) with 0.5um emitter width and 2 um emitter-emitter pitch. The vertical process is an enhanced version of Agilent's 10 GHz ft, 40GHz fmax Micropower process employing self-align stepper lithography, shallow implanted Arsenic emitter, interdigitated TiW-Au metalized fingers and nitride passivation. The material is As epi on <111> silicon(Sb) substrate. The chip size is 300um x 300um. The device used has 40 emitters with emitter length of 15 um. The base junction depth is 1000 Angstroms and the emitter depth is 700A. MAG at 4 GHz was about 16 dB. A commercially available silicon hyperabrupt varactor diode was selected for its linearity and high-Q performance. A Q of >1400 was measured at 50 MHz and capacitance ratio of 3 was measured from 1 to 10V.

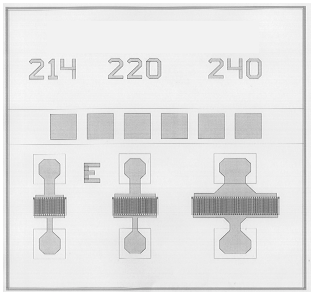

Fig. 3. Low Noise Silicon Bipolar Device

A common-collector configuration was selected due to its inherent instability, minimum parasitic in the resulting circuit layout and lower noise compared to common-base or common-emitter circuits. Agilent Technologies ADS software was used to model the oscillator using Harmonic Balance techniques. Figure 4 shows the oscillator configuration. A high Q microstrip was used as a resonating element at the desired frequency. The length of the high Q resonator was determined meeting the oscillation conditions at the desired final frequency.

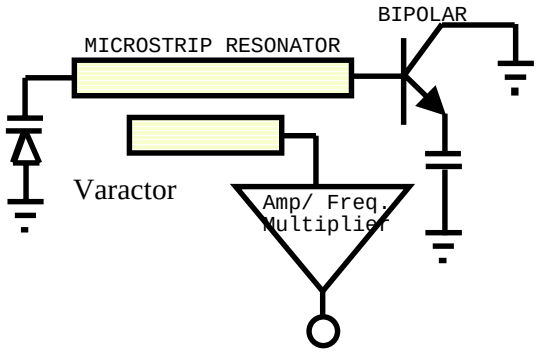

Fig.4 Simplified Oscillator Configuration.

Varactor diode was lightly coupled to the resonating element in order to minimize the impact on the phase noise. The frequency-tuning requirement is limited to the frequency variation of the oscillator under all conditions of parameter variation. A negative temperature coefficient capacitor is used in order to minimize the temperature variation. RF output is coupled lightly from the resonator circuit. This not only allows isolating the oscillator from load fluctuations but also reduces the impact on the phase noise.

For the 10GHz VCO the coupled output port feeds a Agilent GaAs FET MMIC amplifier R271 which offers >10 dB gain and >13 dBm P-1 dB up to 12 GHz. An attenuator in the output is used to achieve the desired output power as well as to improve the output match.

Sources at 20GHz and 40GHz:

Stable frequency sources are required at 20GHz and 40GHz for use in the OC-768 or STM-256 high-speed optical fiber communications systems. Commercially available MMIC multiplier/amplifier can be effectively used to generate low noise signals at 20GHz and 40GHz. Agilent Technologies HMMC-5023 and HMMC-5040 were used as frequency doubler and frequency quadrupler to achieve 20Ghz and 40Ghz signals respectively. These simplified designs require only a bandpass filter after the MMICs to control the sub-harmonically related spurious to a desired level.

The MMICs used are wideband multi-stage amplifiers which become effective multipliers through proper biasing of the first stage [5]. Establishing the bias conditions depends on the application details including fundamental frequency, desired multiple frequency, input drive conditions, output signal level, suppression required etc.

V. PRACTICAL REALIZATION AND RESULTS

The circuit was realized on a 0.25" x 0.25" x .01" alumina substrate using thin film technology. Bipolar transistor was operated at a bias of 8Volts and 25 mA. The capacitance required in the emitter circuit was realized using microstrip distributed capacitance. Two VCOs were realized, one for the standard OC-192 and other for the systems with 7% FEC (Forward Error Correction). The VCOs were tested in a TO-8 package and key results are shown in Table I.

TABLE I

Parameter	*Standard*	*With FEC*	*Unit*
Center Frequency	9.953	10.65	GHz
Power Out	7	7	dBm
Tuning Sensitivity	4 to 6	4 to 6	MHz/V
Tuning Voltage	1 to 10	1 to 10	Volts
Phase Noise @100K	-113	-112	dBc/Hz
Frequency Drift over 0 to 70 deg C	15	15	MHz

Second and Third harmonics were measured to be better than –30 dBc. Output return loss was less than 15 dBr.

Fig. 5 shows the phase noise plot measured using Agilent E5504B phase noise test equipment. Jitter from 50KHz to 80 MHz was calculated to be less than 1mUI. Compared to a typical fundamental VCO, this phase noise represents greater than 15 dB improvement [4].

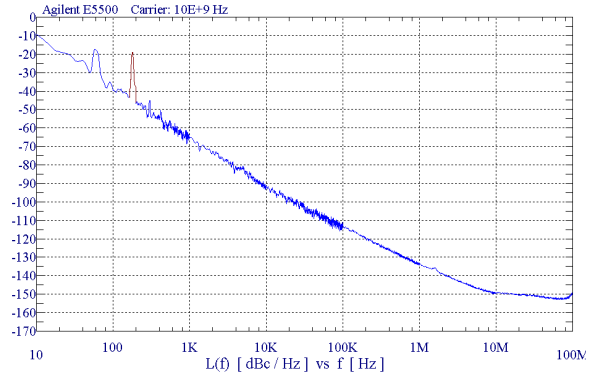

Fig.5 Phase Noise Plot at 9.95 GHz

This oscillator was used as the fundamental oscillator for the 20 and 40 GHz sources. PHEMT Agilent MMICs HMMC-5023 and HMMC-5040 were used as frequency doubler and quadrupler and a bandpass filter was used to reduce the harmonics and sub-harmonics. The impact on the phase noise was measured to be between 6 and 7 dB for the doubler and about 12 dB for the frequency quadrupler. The phase noise plot of the 43 GHz VCO is shown in figure 6. The jitter from 50KHz to 80 MHz at 43 GHz was calculated to be 1.02 mUI = 24 femtosecs or 6.42 mrad rms.

The second harmonic of the 20GHz VCO was measured to be -35 dBc and sub-harmonically related products at 10GHz and 30GHz were measured to be less than –45 dBc. The important parameters of the VCOs for 40Gb/s systems are reported in the table II below:

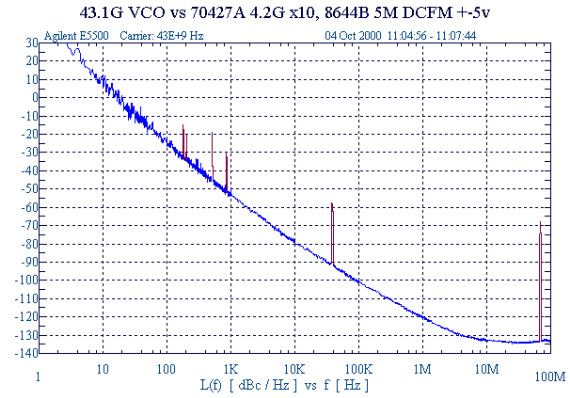

Fig. 6 Phase noise of a 43 GHz VCO

TABLE II

Parameter	*20G*	*40G*	*Unit*
Center Frequency	21.3	42.6	GHz
Power Out	6	6	dBm
Tuning Sensitivity	8 to 12	16 to 24	MHz/V
Tuning Voltage	1 to 10	1 to 10	Volts
Phase Noise @100K	-106	-100	dBc/Hz
Frequency Drift over 0 to 70 deg C	25	50	MHz

VI. CONCLUSION

We have demonstrated low noise microstrip VCOs in thin film using mature technologies of Silicon and GaAs PHEMT to achieve the phase noise required by the modern high performance high-speed communication systems. The obtained phase noise value of –113 dBc/Hz at 100KHz for a planar 10GHz VCOs is the best phase noise value reported till date.

V. ACKNOWLEGEMENTS

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